AMENDMENTS TO THE CLAIMS

1. (Currently amended) A semiconductor device package (10, 100) comprising:

a molding compound (18) forming a portion of:

a first package face (14),

a second package face (12) opposite the first package face (14), and

package side faces (16) extending between the first and second package faces (14, 12);

a semiconductor device (20) at least partially covered by the molding compound (18), the semiconductor device (20) including a plurality of I/O pads (38); and

an electrically conductive lead frame (22) comprising:

a plurality of posts (24) disposed at a perimeter of the package (10, 100), each post (24) having a first contact surface (26) disposed at the first package face (14) and a second contact surface (28) disposed at the second package face (12), the semiconductor device (20) being positioned in a central region defined by the plurality of posts (24), and

a plurality of post extensions (32), each post extension (32) having a third contact surface (34) disposed at the second package face (12), the plurality of post extensions (32) extending from the plurality of posts (24) toward the semiconductor device (20), each of the post extensions (32) including a bond site (36) formed on a surface of the post extension (32) opposite the second package face (12), at least one of the I/O pads (38) being electrically connected to the post extension (32) at the bond site (36),

wherein

the molding compound (18) is coplanar with side surfaces (60) of the posts (24) at the package side faces (16), and

two package side faces (16) meet to form a square corner at each of four corner regions of the package (10, 100).

2. (Original) The semiconductor device package (10) of claim 1, wherein the at least one of the I/O pads (38) is wire bonded or tape bonded to the bond site (36).

3. (Original) The semiconductor device package (10) of claim 2, wherein the die (20) is attached to a support pad (30), the support pad (30) including a surface extending along the second package face (12).

4. (Withdrawn) The semiconductor device package (100) of claim 1, wherein the at least one of the I/O pads (38) is directly electrically connected to the bond site (36) for forming a flip-chip type connection.

5. (Original) The semiconductor device package (10, 100) of claim 1, wherein the semiconductor device package (10, 100) has four package side faces (16), and the plurality of posts (24) are disposed among two of the four package side faces (16).

6. (Original) The semiconductor device package (10, 100) of claim 1, wherein the semiconductor device package (10, 100) has four package side faces (16), and the plurality of posts (24) are disposed among all of the four package side faces (16).

7. (Withdrawn) A stack of semiconductor device packages (10, 100), each semiconductor device package (10, 100) comprising:

a molding compound (18) forming a portion of:

a first package face (14),

a second package face (12) opposite the first package face (14), and

package side faces (16) extending between the first and second package faces (14, 12);

a semiconductor device (20) at least partially covered by the molding compound (18), the semiconductor device (20) including a plurality of I/O pads (38);

an electrically conductive lead frame (22) comprising:

a plurality of posts (24) disposed at a perimeter of the package (10, 100), each post (24) having a first contact surface (26) disposed at the first package face (14) and a second contact surface (28) disposed at the second package face (12), the semiconductor device (20) being positioned in a central region defined by the plurality of posts (24), and

a plurality of post extensions (32), each post extension (32) having a third contact surface (34) disposed at the second package face (12), the plurality of post extensions (32) extending from the plurality of posts (24) toward the semiconductor device (20), each of the post extensions (32) including a bond site (36) formed on a surface of the post extension (32) opposite the second package face (12), at least one of the I/O pads (38) being electrically connected to the post extension (32) at the bond site (36);

wherein the first contact surfaces (26) of at least one of the semiconductor packages (10, 100) is directly electrically connected to one of the first and second contact surfaces (26, 28) of an adjacent semiconductor package (10, 100).

8. (Withdrawn) The stack of semiconductor device packages (10) of claim 7, wherein the at least one of the I/O pads (38) is wire bonded or tape bonded to the bond site (36).

9. (Withdrawn) The stack of semiconductor device packages (10) of claim 8, wherein the semiconductor device (20) is attached to a support pad (30), the support pad (30) including a surface extending along the second package face (12).

10. (Withdrawn) The stack of semiconductor device packages (100) of claim 7, wherein the at least one of the I/O pads (38) is directly electrically connected to the bond site (36) for forming a flip-chip type connection.

11. (Withdrawn) The stack of semiconductor device packages (10, 100) of claim 7, wherein each semiconductor device package (10, 100) has four package side faces (16), and the plurality of posts (24) are disposed among two of the four package side faces (16).

12. (Withdrawn) The stack of semiconductor device packages (10, 100) of claim 7, wherein each semiconductor device package (10, 100) has four package side faces (16), and the plurality of posts (24) are disposed among all of the four package side faces (16).

13. (Withdrawn) A method for use in manufacturing a semiconductor device package (10, 100), the method comprising:

forming a plurality of posts (24) from an electrically conductive material, the plurality of posts (24) having a profile height equal to a predetermined height of the semiconductor device package (10, 100), and each post (24) in the plurality of posts (24) having a side surface (60) positioned at a predetermined package side face (16);

disposing a semiconductor device (20) within a central region defined by the plurality of posts (24), the semiconductor device (20) including a plurality of I/O pads (38) disposed thereon;

electrically connecting the plurality of I/O pads (38) to associated bond sites (36) formed on electrically conductive post extensions (32) protruding from the plurality of posts (24);

covering at least a portion of the semiconductor device (20), the plurality of posts (24), and post extensions (32) with a molding compound (18).

14. (Withdrawn) The method of claim 13, wherein forming the plurality of posts (24) includes: selecting a sheet of the electrically conductive material having a profile height equal to the predetermined profile height of the semiconductor device package (10, 100); and selectively removing material from the sheet to form the posts (24).

15. (Withdrawn) The method of claim 14, wherein forming the plurality of posts (24) includes:

selecting a sheet of the electrically conductive material having a profile height greater than the predetermined profile height of the semiconductor device package (10, 100), and

selectively removing material from the sheet to form the posts (24) on a substrate portion (76) of the electrically conductive material;

and wherein the method further comprises:

after covering the semiconductor device (20), the plurality of posts (24), and the post extensions (32) with the molding compound (18), removing the substrate portion (76) of the electrically conductive material.

16. (Withdrawn) The method of claim 13, wherein electrically connecting the I/O pads (38) to the bond sites (36) includes: wire bonding or tape bonding the I/O pads (38) to the bond sites (36).

17. (Withdrawn) The method of claim 13, wherein electrically connecting the I/O pads (38) to the bond sites (36) includes: directly soldering the I/O pads (38) to the bond sites (36) to form a flip-chip type connection.

18. (Withdrawn) The method of claim 13, further comprising: forming a contact surface (26, 28) on an end of each of the posts (24); and directly electrically connecting the contact surface (26, 28) to a contact surface (26, 28) on an adjacent semiconductor device package (10, 100).